



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: William K. Stewart, Charles W. Selvidge, Kenneth Crouch, Marina Wong and Mark Seneski

Application No.: Group Art Unit:

Filed: March 12, 2001 Examiner:

Title: LOGIC ANALYSIS SYSTEM FOR LOGIC EMULATION SYSTEMS

Date: 3-12-01

EXPRESS MAIL LABEL NO. EL 55228288945

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This Information Disclosure Statement is submitted:

☐ under 37 CFR 1.129(a), or
(First/Second submission after Final Rejection)

☒ under 37 CFR 1.97(b), or
(Within any one of the following time periods: three months of filing national application (other than a CPA) or date of entry of the national stage in an international application; or before the mailing date of a first office action on the merits in a non-provisional application, including a CPA, or a Request for Continued Examination).

☐ under 37 CFR 1.97(c) together with either:
☐ a Statement under 37 CFR 1.97(e), as checked below, or
☐ a \$180.00 fee under 37 CFR 1.17(p), or
(After the 37 CFR 1.97(b) time period, but before final action or notice of allowance, whichever occurs first)

☐ under 37 CFR 1.97(d) together with:
☐ a Statement under 37 CFR 1.97(e), as checked below, and
☐ a \$180.00 fee under 37 CFR 1.17(p), or
(Filed after final action or notice of allowance, whichever occurs first, but on or before payment of the issue fee)

☐ under 37 CFR 1.97(i):
Applicant requests that the IDS and cited reference(s) be placed in the application filewrapper.
(Filed after payment of issue fee)

Statement Under 37 CFR 1.97(e)

Statement Under 37 CFR 1.97(e)

- ☐ Each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement; or
- ☐ No item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned, after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of this Information Disclosure Statement.

Statement Under 37 CFR 1.704(d) (Patent Term Adjustment)

- ☐ Each item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in § 1.56(c) more than thirty days prior to the filing of the Information Disclosure Statement.
- ☒ Enclosed herewith is form PTO-1449:
- ☐ Copies of the cited references are enclosed.
- ☒ Copies of cited references are enclosed except those entered in prior application, U.S. Application No. 09/133,959, to which priority under 35 U.S.C. 120 is claimed. The earlier application contains copies of the cited references.
- ☐ The listed references were cited in the enclosed International Search Report in a counterpart foreign application.

Concise Explanation Requirement (non-English references):

- ☐ The "concise explanation" requirement for reference(s) [] under 37 CFR 1.98(a)(3) is satisfied by:
- ☐ the explanation provided on the attached sheet.
- ☐ the explanation provided in the Specification.
- ☐ submission of the enclosed International Search Report.
- ☐ the enclosed English language abstract.

- ☐ Applicant requests that the following pending applications be considered:

Examiner's
Initials

____ U.S. Patent Application No. [], Publication No. [], Publication Date [],
by [inventor(s)], filed [], Docket No.: []

____ U.S. Patent Application No. [], Publication No. [], Publication Date [],
by [inventor(s)], filed [], Docket No.: []

____ U.S. Patent Application No. [], Publication No. [], Publication Date [],
by [inventor(s)], filed [], Docket No.: []

Examiner_____
Date

- ☐ A copy of each above-cited application, including the current claims, is enclosed, except those entered in prior application, U.S. Application No. [], to which priority under 35 U.S.C. 120 is claimed. [The earlier application contains copies of the application, including the current claims.]

The Examiner is requested to return a copy of the above list of pending applications indicating which references were considered with the next office communication.

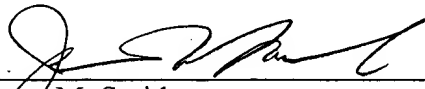
It is requested that the information disclosed herein be made of record in this application.

Method of payment:

- ☐ A check for the fee noted above is enclosed, or the fee has been included in the check with the accompanying Reply. A copy of this Statement is enclosed.
- ☐ Please charge Deposit Account 08-0380 in the amount of \$[]. A copy of this Statement is enclosed.
- ☒ Please charge any deficiency in fees and credit any overpayment to Deposit Account 08-0380.

Respectfully submitted,

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Dated: 3/9/11

PTO-1449 REPRODUCED				ATTORNEY DOCKET NO. 1892.1003-002		APPLICATION NO.	
INFORMATION DISCLOSURE CITATION IN AN APPLICATION March 7, 2001 (Use several sheets if necessary)				APPLICANT William K. Stewart et al.			
				FILING DATE 3/12/01		GROUP	
U.S. PATENT DOCUMENTS							
EXAM- INER INI- TIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE IF APPROPRIATE
AA		4,541,100	09/10/85	Sutton et al.	375	10	
AB		4,782,461	11/01/88	Mick et al.	364	900	
AC		4,857,774	08/15/87	El-Ayat et al.	307	465	
AD		5,109,353	04/28/92	Sample et al.	364	578	
AE		5,425,036	06/13/95	Liu et al.	371	23	
AF		5,475,624	12/12/95	West	364	578	
AG		5,513,338	04/30/96	Alexander et al.	395	500	
AH		5,548,794	08/20/96	Yishay et al.	395	871	
AI		5,572,710	11/05/96	Asano et al.	395	500	
AJ		5,596,742	01/21/97	Agarwal et al.	395	500	
AK		5,680,592	10/21/97	Priem	395	527	
AA2		5,802,348	09/01/98	Stewart et al.	395	500	
AB2		5,418,452	05/23/95	Pyle	324	158	
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION YES NO
	AL						
	AM						
	AN						
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)							
	AR	Babb, J., et al., "Virtual Wires: Overcoming Pin Limitations in FPGA-based Logic Emulators," <i>IEEE</i> , 142-151 (1993).					
	AS	Jones, D and Lewis, D.M., "A Time-Multiplexed FPGA Architecture for Logic Emulation," <i>IEEE</i> , Custom Integrated Circuits Conference, 495-198 (1995).					
	AT	Babb, J., et al., "Logic Emulation with Virtual Wires," <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 16(6): 609-626 (1997).					
EXAMINER				DATE CONSIDERED			

J0972 U.S. PTO
 09/804504
 03/12/01